REMARKS

Claims 1-4 and 13-21 are now pending in the application, with claims 1, 20 and 21 being the independent claims. Claims 5-12 have previously been canceled. Claims 1-4 and 13-21 have been amended. Support for the amendments is found in the application as originally written. For example, support for "a DV video signal" and a "second video signal" is found, *inter alia*, at paragraph [0016]. Therefore, it can be seen that no new matter has been added.

Claims Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1-4 and 13-21, all the pending claims, under 35 U.S.C. § 103(a) as being obvious in light of a combination of Stallkamp (US Patent No. 6,895,009 B1) and Domon (US Publication No. 2003/0014679 A1. Reconsideration is respectfully requested. Independent claims 1, 20 and 21 have been amended to recite a video signal conversion system that includes, in pertinent part, a first node and a second node in which one of the first node and the second node serves as a cycle master, the first node having a DV data processing unit configured to transmit a DV video signal to the second node via the IEEE1394 bus at a transfer rate synchronized with a cycle start packet output from the cycle master and the second node has a data conversion unit configured to receive a first DV video signal from a DV data processing unit of the first node via an IEEE1394 bus, convert the first DV video signal to a second video signal, and output the second video signal generated by conversion of the first DV video signal image data in the second node in synchronism with an external reference signal. Claim 20 additionally recites that the second video signal is an analog video signal, while claim 21 additionally recites that the second digital video signal image data is a second video signal in SDI format. Applicants have discovered that by synchronizing the data transfer from the first node with the output of converted data from the second mode, it is possible to convert video signals in real time while preventing image defects such as dropped frames or repeated frames in the converted video signals. (Abstract.) .

Stallkamp relates to a much different system. Stallkamp does not disclose, nor would it have suggested, a system in which a second node has a data conversion unit configured to convert a first DV video signal to a second video signal, and output the second video signal image data generated by conversion of the first DV video signal image data in the second node in synchronism with an external reference signal. The only conversion disclosed in Stallkamp is conversion by a frame rate converter. (Stallkamp, col. 5, lines 57-67.) *A fortiori*, Stallkamp does not disclose, nor would it have suggested, a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal, such that the transfer of the first DV video signal to the second node is synchronized with the output of the second video signal from the second node.

Nothing in the teachings of Domon, whether considered alone, or together with Stallkamp, makes up for these deficiencies. Domon is cited merely because it discloses that the first data is a video signal in DV format and a the second data is an analog video signal or SDI video signal (page 5, Office Action of October 27, 2012) and that the first node is configured to transmit first data to a second node at a transfer rate synchronized with a cycle start packet out put from the master cycle (page 5, Office Action of October 27, 2012). However, nothing in Domon whether considered alone, or together with Stallkamp would have suggested, *inter alia*,. a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal, such that the transfer of the first DV video signal to the second node is synchronized with the output of the second video signal from the second node. Therefore, the rejection of independent claim 1, its dependent claims 2-4 and 13-19, independent claim 20 and independent claim 21 under 35 U.S.C. § 103(a) in light of the proposed combination of references should be withdrawn.

CONCLUSION

Therefore, in view of the above amendment and remarks, the Applicant respectfully submits that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. As such, allowance of the above Application is requested. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call the Applicant's attorney at the number listed below.

Respectfully submitted,

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By: /Jeffrey F. Craft/
Jeffrey F. Craft, Reg. No. 30,004
Telephone: 213-629-7400

Customer No. 68543
Arent Fox LLP
555 West Fifth Street, 48th Floor
Los Angeles, CA 90013
United States of America
Telephone No. (213) 629-7400
Facsimile No. (213) 629-7401